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RADAR HANDBOOK

Editor in Chief
MERRILL I. SKOLNIK

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Examples of Phase Detectors

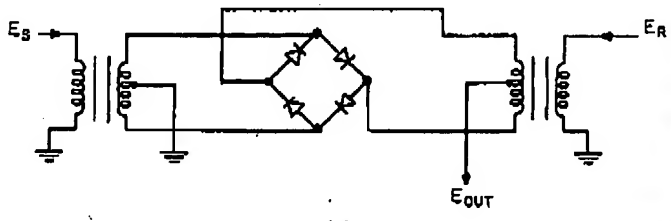
Multiplier Detector. The gated-beam tube and, to some extent, the beam-deflection tube have been used as analog multipliers to obtain the product of the signal and reference waveforms. They are self-limiting and produce a gradual transition from the *I* to "*I*" characteristics about the saturation level. When they are used as synchronous detectors, the dynamic range is restricted by the high noise level of these devices. This type of multiplier detector also may be implemented by using a field-effect transistor (FET) multiplier as suggested by Highleyman and Jacob.[12]

Balanced-Diode Detector. The balanced-diode detector of Fig. 3.19*a* is widely used because of its unusually favorable characteristics. When two sinusoids of frequency ω and phase difference θ are applied to this detector, the output is given by

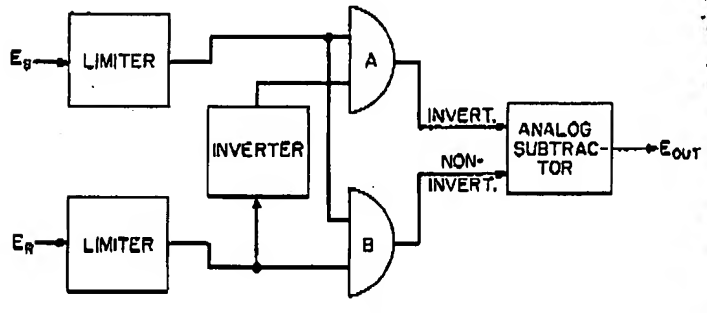
$$E_{out} = K(\cos\theta - \cos 2\omega t + \text{higher-order terms}) \tag{3.24}$$

Under these conditions, the characteristic is sinusoidal, and the ripple is free from a fundamental component. When bandwidth permits, the detector will operate with square-wave inputs to give a triangular characteristic.

This circuit can be purchased in modular form, containing a pair of balanced wideband transformers and matched hot-carrier diodes. The detector can be obtained with 35 dB isolation between ports over a frequency range of 3 to 100 MHz. Units having a maximum frequency limit of 1 GHz are available.



(a)



(b)

FIG. 3.19 (*a*) Balanced-diode detector. (*b*) Coincidence phase detector.

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In theory, the dynamic range is determined by the maximum signal-to-noise ratio at the output. In practice, however, it tends to be limited by unbalanced residuals and their fluctuation. Very precise detectors of this type may have a usable dynamic range of 50 dB.

Coincidence Phase Detector. The coincidence detector of Fig. 3.19*b* provides a triangular output characteristic. When E_S and E_R are in phase, AND gate *B* registers coincidence half the time, and AND gate *A* registers no coincidence. This condition leads to maximum negative output. When E_S and E_R are out of phase, the reverse condition exists, and maximum positive output results. Normally the triangular characteristic exhibits some rounding of the peaks. However, the detector has been built with very sharp peaks, using a tunnel-diode threshold in each channel.

The coincidence phase detector has a fundamental ripple-frequency component. A higher ripple frequency results from exclusive OR-gate logic, but this introduces voltage offsets that may be troublesome.

Analog-to-Digital Phase Detector. The phase detector of Fig. 3.20 measures the time interval between positive (or negative) zero crossings of the signal and reference waveforms. A pair of zero-crossing detectors generate sharp spikes at their respective points of crossing. The reference-channel spike sets a RESET-SET (*R-S*) flip-flop, and the signal-channel spike resets it. A gated oscillator generates a clock waveform while the flip-flop is in the SET state, and a counter measures the length of this interval. Filtering is accomplished by a buffer register.

The resolution of this phase detector is determined by the ratio of the clock frequency to the intermediate frequency ω_2 of the signal. In a tracking radar with a range gate, the signal bandwidth may be narrowed drastically after gating with-

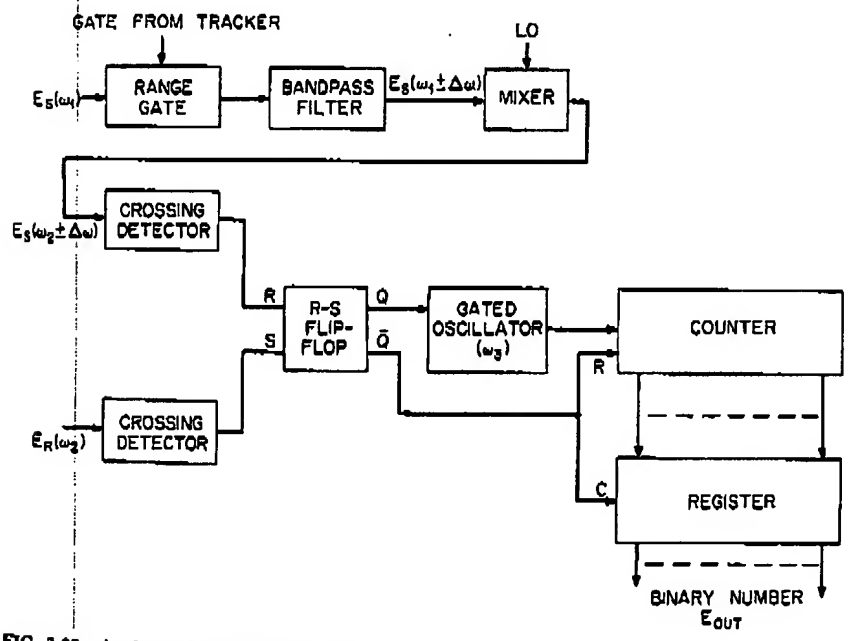
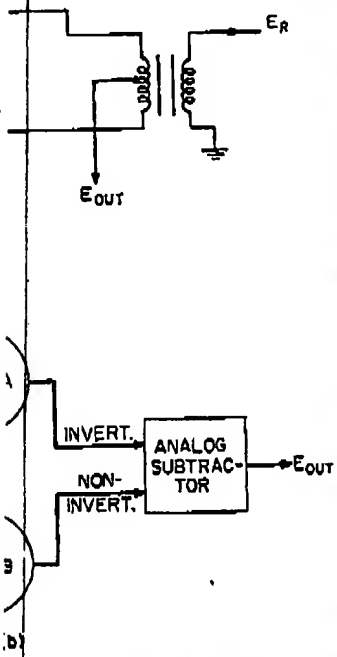


FIG. 3.20 Analog-to-digital phase detector.



b) Coincidence phase detector.